A study of temperature field in a GaN Heterostructure Field-Effect Transistor

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ABSTRACT: We propose in this paper a three-dimensional finite element based heat transfer model for a Gallium Nitride-based Heterostructure Field-Effect Transistor (henceforth referred to as GaN HFET). Analyses were carried out to study the distribution of temperature in the HFET under steady state conditions for two different steady-current inputs. Two different substrates for the HFET, sapphire and silicon carbide (SiC), were studied. The paper discusses the effect of using a heat sink and also that of using reasonable contact resistances on the substrate side of the HFET, on the temperature profile. In all cases, the gate region of the HFET was found to attain the highest temperature. Subsequent experiments to validate the results of the computational analysis were carried out at the Oakridge National Laboratories, Knoxville, and are also presented in this paper.

1 INTRODUCTION

Heating in electronic devices is one of the prime factors that limits their performance. With the ever-increasing level of integration and the resulting high power densities, there is a constant need to study and devise ways of dissipating the heat produced, in order to keep up the present rate of development. GaN based HFET devices offer the potential of high-power, high-speed and high-temperature performance better than that of Si and GaAs based devices. High-temperature performance of AlGaN/GaN HFETs grown on SiC substrates has been found to be much better than the performance with sapphire substrates (Gaska et al. 1997). Gaska et al. (1998) have also reported that heat dissipation strongly affects the device characteristics soon after the application of source-drain voltage. Irreversible degradation of device performance of AlGaN/GaN FETs caused by loss in channel current between 600 °C and 800 °C has been reported (Daumiller et al. 1999).

The schematic of a typical GaN HFET with its approximate dimensions is shown in Figure 1.

Figure 1. Schematic of a typical GaN HFET
It consists of an SiC substrate, on top of which layers of different materials are grown. SiC and GaN have different crystal structures and growing GaN directly over SiC results in cracks at the interface owing to the lattice mismatch. Therefore, an AlN layer is first grown on the SiC. The AlN layer aids in the nucleation of GaN. A thin layer of highly conducting AlGaN is grown over the GaN layer. Most of the current flow is concentrated in this layer. Current flows between the source and the drain. Applying a voltage across the gate can regulate the flow of this current. The flow of current causes the transistor to heat-up. The temperature is found to be maximum in the region around the gate. An attempt was made to simulate the effects of using different substrates, with and without a heat sink, for two different power inputs. This analysis was carried out in ABAQUS/Standard. MSC PATRAN 8.5 was used as the pre-processor and the model was post-processed in ABAQUS 5.8-16. ABAQUS is a tried and tested software that has been used extensively over the years for structural and thermal analysis (Khan et al. 1999), thus justifying it’s choice in our case.

In order to simplify the numerical computations, analysis was carried out on a symmetric half of the transistor, bisected by a vertical plane through the middle of the device parallel to its depth. The face of the HFET thus exposed was made insulated. The smallest linear dimension acceptable to the program was found to be around 0.2\( \mu \)m. The smallest linear dimension in the actual transistor was about 0.01\( \mu \)m. As a result, some of the actual smaller dimensions had to be modified to accommodate this limitation. SiC was used as the substrate below which a layer of gold was attached to enhance the heat sinking. Henceforth, we will be referring to this layer of gold as the heat sink. The heat sink was maintained at a constant temperature of 25°C. The main underlying motivation was to obtain data that would provide an insight into the larger problem of managing heat at the device level itself.

2 EXPERIMENTAL ANALYSIS

Experiments were carried out at the Oakridge National Laboratories, Knoxville, Tennessee. ImageDesk II\textsuperscript{TM}, a Pentium PC hosted desktop image acquisition, processing, and analysis system, interfaced with Amber’s Galileo imaging IR camera, was used to acquire a sequence of images of similar transistors that were powered to different levels. The Raytheon/Amber Galileo (Radiance HS) is a 12-bit IR camera (the digital output has a 12-bit dynamic range), which uses a cooled InSb 256x256 focal plane array as a detector. In snapshot mode the camera allows stop-action analysis of events as short as 2\( \mu \)s. Working in the 3-5\( \mu \)m spectral range, it monitors temperatures within a wide range at a resolution of 12 bits (Krehl et al. 1999). Favro et al. (2001) have reported using this camera for sonic IR imaging of cracks and delaminations. In order to obtain a microscopic resolution of the temperature distribution within the HFET, the thermographic camera was coupled to a 4X infrared sensitive objective, which allowed a spatial resolution of about 5\( \mu \)m. Figure 2 shows a snapshot of the HFET under steady-state conditions as taken by the camera. The calibration curve correlating the camera count values (proportional to the intensity of emitted IR radiation) with the actual temperatures is shown in Figure 3.

3 GOVERNING EQUATIONS

Basic energy balance equations were used in the computational analysis. Free convection was assumed to take place at the free surfaces. An explanation of the symbols used is given below:

- \( n \) = each of the three coordinate axes x, y and z
- \( \alpha \) = thermal diffusivity
- \( k \) = thermal conductivity, \( h \) = convection coefficient
**Ts** = Surface temperature  
**T∞** = Ambient temperature  
• **q** = Heat generation per unit volume of the gate material = Power input to the HFET per unit volume of the gate

3.1 Conduction  
For each of the interior elements, the governing equation at any instant **t** is

\[
\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = \frac{1}{\alpha} \frac{\partial T}{\partial t}
\]

3.2 Convection at the surface elements

\[
k \frac{\partial T}{\partial n} = h(T_s - T∞)
\]

3.3 Heat generation at the gate

\[
\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{\dot{q}}{k} = \frac{1}{\alpha} \frac{\partial T}{\partial t}
\]

4 COMPUTATIONAL ANALYSIS

As mentioned earlier, the finite-element analysis was conducted on a half-section of the device. An isometric view of the model is shown in Figure 4. The geometry actually modeled was a simplified form of the schematic discussed earlier. The model consisted of three layers: the substrate (sapphire or SiC), a GaN layer and an AlGaN layer. Gold was used as the material for the source and for the sink. The objective was to obtain the temperature gradients in the x and y co-ordinate directions.

Figure 2. Thermographic image of an HFET when powered up.  
Figure 3. Calibration curve used to relate IR counts to temperature.
The device was assumed to be very long in the z direction. The figure above shows a steady-state maximum temperature of 282°C, which is in the region of the gate, for a heat flux of 8x10^7 W/m^2 and an SiC substrate. A layer of gold was used as a heat sink and was maintained at 25°C, which is the minimum temperature in the figure. Figure 5, which is a magnified front view, gives a clearer picture of the temperature maps.

Two types of cases were simulated: one with a heat sink and the other without one. The choices of these cases was driven by the motivation to simulate the temperature distribution in the transistor for an actual case using different substrates, and then predict the distribution for a case with additional heat sinking.

4.1 Case 1: Analysis with no heat sink

A very high value for the convective coefficient was applied to the bottom surface of the substrate. A value of 25,000 W/m^2 °C was chosen, based on the values recommended by Incropera & DeWitt (1996). As in the case with heat sink, sapphire and SiC were used as the substrates and the same conductivity values were used. The same boundary conditions were also applied.

4.2 Case 2: Analysis with heat sink

A thin layer of gold was added to the bottom of the substrate to act as a heat sink. The sink was maintained at a constant temperature of 25°C. The surface of the transistor parallel to the yz plane and adjoining the gate was thermally insulated. A heat flux was applied to the gate and convective boundary conditions were applied to all remaining exposed surfaces. The case with no convective boundary conditions applied was also considered. Sapphire and SiC were used as the substrates. Typical values of thermal conductivity of sapphire and SiC at room temperature are 25-50 W/m°C (Cooke 1993) and 500W/m°C (Morkoc et al. 1994), respectively. A conductivity value of 40 W/m°C was used for sapphire. In case of SiC, a value of 490 W/m°C was used for a very pure material while a general value of 300 W/m°C was used for ordinary SiC.
5 RESULTS

First, the experimental results are compared with those obtained from simulation. For an input power of 0.75W, the temperature against time plot from the experiment is shown in Figure 6. The two peaks represent the temperatures at the two gates. The average peak temperature is seen to be around 140°C. The accuracy of these results was limited by the resolution of the lenses used to obtain the thermographic data. The FEM simulation of this experiment predicted similar results (Figure 7). The model did not include a heat sink. Instead, a contact resistance approximated by an $h$ value of 12,500 W/m²°C was applied to the base of the SiC substrate, with conductivity of SiC taken as 490 W/m°C.

Although the peak temperature obtained from simulation corresponds closely to the actual peak temperature for the given value of the convective coefficient, a temperature gradient of only about 5° was a lot different from the gradient of around 50° to 55° plotted from the experimental data. This points to inherent defects in the simplifications done in the model. The presence of a temperature gradient seems to suggest that the assumption of a heat sink may be more reasonable than that of a contact resistance at the substrate base. Also, it is difficult to determine accurately the thermal conductivity of SiC, as it seems to be a strong function of the level of impurity. Thus, there is almost certainly an offset between the conductivity value we used and the actual value. Later in the paper we discuss how the thermal conductivity of SiC may affect the overall heat transfer process.

In order to simplify the analysis, the transistor was assumed to be exposed to the ambient, except at the base, where a contact resistance was assumed. This assumption may not correctly represent the actual scenario of the experiment where the device that was tested was surrounded by other devices. At a given time only one device was powered up.

6 PARAMETRIC STUDIES

Studies were carried out to see the effects on heat transfer of the following parameters:

(i) Different materials and properties for the substrate with no heat sink.
(ii) Heat sink attached to the substrate.

Sapphire and SiC were used as the substrates. In case of SiC, two different values for the conductivity, corresponding to those of impure and pure SiC, were used. Cases with no heat sink
attached were also studied. Figure 8a below shows the temperature variation along the x-axis for a heat flux $4 \times 10^9$ W/m² and a heat sink maintained at 25°C. As can be seen, the highest temperature is obtained in the gate region. Another noticeable aspect is the existence of a temperature gradient. For a sapphire substrate, the peak temperature was about 700°C. The peak temperature was found to be significantly lower when SiC was used as the substrate. As seen in Figure 8b, for an SiC conductivity of 300 W/m°C, it was about 190°C while for a conductivity of 490 W/m°C the highest temperature was around 150°C.

Figure 8a. Variation of temperature along the x-axis for a heat flux of $4 \times 10^9$ W/m² with a heat sink maintained at 25°C.

Figure 8b. Magnified view of a portion of Figure 8a showing the variation of temperature near the gate for two different thermal conductivities of SiC.

Thus, it can be inferred that the thermal conductivity of the substrate seems to have a significant bearing on the peak temperature. This has been shown to be true experimentally (Gaska et al. 1998). Figures 9a and 9b show the results obtained for the same power input, but with no heat sink attached. Instead, an $h$ value of 25,000 W/m² °C was applied to the base of the substrate. The temperatures obtained were extremely high. The peak temperature approached 2300°C at the gate for Sapphire. For SiC, the temperatures were close to 1800°C for a conductivity of 300 W/m°C and 1750°C for a conductivity of 490 W/m°C.

Figure 9a. Temperature graph along the x-axis for a heat flux of $4 \times 10^9$ W/m², with a contact resistance applied to the substrate base instead of a heat sink.

Figure 9b. A closer view of the region of the plot in Fig. 9a showing the temperature variation near the gate.
These temperatures are much above the Debye temperature for GaN, which is about 750°C (Manasreh 1997). The Debye temperature may be used as a criterion for the mechanical and chemical stability of semiconductor materials (Daumiller et al. 1999). Thus, beyond 750°C, GaN would become unstable. Next, an analysis with a heat sink was done for a heat flux of $8 \times 10^9$ W/m². The results obtained are presented in Figures 10a and 10b.

### 7 CONCLUSION

A 3-D finite-element-based model was proposed to simulate the temperature distribution in GaN based HFETs. Data obtained from experiments performed at the Oakridge National Lab. and those obtained from the simulated analysis agreed on the peak temperature reached for the given power input. In both cases, this temperature was found to occur in the region of the gate. But the simulation did not predict the temperature gradient as found in the experimental analysis. As a result, some of the assumptions and simplifications made while developing the model would need re-evaluation.

A number of conclusions can be drawn from the parametric studies carried out. These studies confirm the fact that SiC, owing to its higher thermal conductivity, is a much better substrate for GaN-based microelectronic devices than sapphire. Or stated another way, the thermal conductivity of the substrate was found to have a significant effect on the peak temperature attained by the device. Also, the heat sinking from the transistor is predicted to be greatly enhanced by including a layer of a high thermally conducting material (gold was used in our case) right below the substrate, and maintain it at a temperature close to the ambient using some cooling mechanism.

### REFERENCES


